Docket No. 200314976-1

Remarks

This Amendment is responsive to the **June 27, 2007** Office Action. Reexamination and reconsideration of the remaining claims (1-11, and 14-22) is respectfully requested.

Summary of The Office Action

Claims 1-3, 6-11, 14, and 17-20 were rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Cooper et al. (US Patent No. 7,082,542) (Cooper).

Claims 4-5, 15-16, and 22 were rejected under 35 U.S.C. 103(a) as purportedly being unpatentable over Cooper in view of Oshins et al. (US Patent No. 6,980,944 B1)(Oshins).

Claim 21 was rejected under 35 USC 103(a) as being unpatentable over Cooper in view of Bhatia et al. (US Patent No. 6,535,798 B1)(Bhatia).

The disclosure was objected to because the amendment filed 3/22/07 purportedly introduced new matter into the disclosure in contravention of 35 USC 132(a), which states that no amendment shall introduce new matter into the disclosure of the invention unless it is meant solely to facilitate clearing the issue of non-statutory subject matter raised in a previous office action. Applicant clarifies the amendment herein.

The drawings were objected to because the Office Action asserts that figures 1-4 should be designated by a legend such as –Prior Art—because only that which is old is purportedly illustrated. Applicant describes herein why this objection should be removed.

The Office Action states in a Claim Interpretation section that the claim limitation "to produce a simulated processor performance state without causing an actual ACPI processor performance state change" is being interpreted as meaning "where the actual internal frequency of the processor has not been changed (spec [0039]) by throttling a clock signal supplied to the processor (spec [0061]). While the internal state of the processor has not been changed, externally the state of the processor has changed, as the logic establishes the

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desired (simulated) processor performance state by causing the processor to be throttled." Applicant describes herein how this interpretation is not completely accurate.

The Office Action states in the Response to Arguments section that "the language of claims 1-11 while statutory, indicate intended use and thus the limitations are not given patentable weight i.e. "memory to store and address", "logic to select a bit pattern". The Office Action then states that claims 1-11 are fully anticipated by any computer system since claim 1 simply describes an apparatus with a memory and logic. (Office Action, Page 8). Applicant describes herein how the elements and limitations of the logic describe a novel apparatus.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §103

To establish a prima facie case of 35 U.S.C. §103 obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 The teaching or suggestion to make the claimed combination must be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the criterion described in MPEP 2143.03 is not satisfied since the reference does not teach or suggest all the claim limitations. All the independent claims concern simulating a processor performance state without causing an actual ACPI processor performance state change. Cooper does not teach creating a simulated processor performance state without causing an actual ACPI processor performance state change. Instead, Cooper teaches a throttling emulator that **requires** an ACPI processor performance state change. None of the references cure this glaring defect in Cooper. Thus, none of the claims are obvious for at least this reason.

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Independent Claim 1

Claim 1 recites an apparatus that produces a simulated processor performance state **without causing an actual ACPI processor performance state change**. The Office Action asserts that claim 1 is obvious in light of Cooper. However, Cooper does not teach simulating a processor performance state but rather teaches actually changing internal ACPI processor performance states. Cooper recites that "[t]he processor is transitioned to one of the operational state and the low power state according to the processor state." (Abstract).

Cooper actually teaches away from the claimed apparatus. Cooper recites that "throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using throttling.

Having described the horrors of throttling, Cooper then describes an alternative known as "emulating throttling". Column 1, line 54. Emulating throttling includes "transitioning the processor to one of the operational state and the low power state." Column 1, lines 59-61. The throttling emulator includes a throttling state and an Advanced Configuration and Power Interface (ACPI) operating system. Column 4, lines 15-29. The throttling emulator transitions to a low power state by setting a processor to one of the ACPI states C1, C2, C3, and sleep state S1. Column 5, lines 31-39. The throttling emulator transitions to an operational power state by setting a processor to the ACPI state C0. Column 5, lines 40-46. Cooper recites that "the SMI timer handler performs operations to enter the desired low state (Block 440). As discussed above, the low state may be any one of a power state C1, C2, C3, and the sleep state S0. ... The SMI timer handler performs operations to enter the normal operational state (e.g., the C0 state) (block 450)". Column 6, lines 24-46. Cooper unquestionably involves an internal ACPI state change.

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Cooper describes how emulating throttling involves changing an internal ACPI state. This is precisely the limitation that the claim language "without causing an actual ACPI processor performance state change" addresses. All the independent claims require that no ACPI state change happen yet Cooper requires that an ACPI state change happen. Thus, Cooper is exactly opposite to the approach claimed and described. For at least this reason Cooper does not render any of the independent claims obvious.

The Office Action states that Cooper does not explicitly disclose creating the simulated processor performance state without causing an actual ACPI processor performance state change, yet that is exactly what claim 1 describes, creating a simulated processor performance state without causing an actual ACPI processor performance state change. There is a complete disconnect between Cooper and the claim. Cooper changes a state explicitly, the claim does not. The Office Action attempts to sidestep this fundamental flaw when it explains that:

> Although Cooper does not explicitly disclose producing a simulated processor performance state without causing an actual processor performance state change, Cooper does teach throttling a clock signal to the processor where the internal state of the processor has not changed but the external state of the processor has changed by means of throttling emulation (column 6, lines 24-46) and it would have been obvious to an ordinary person skilled in the art at the time of the invention to use Cooper to simulate processor performance states in order to provide the same functional result of simulating processor performance states while providing more flexibility than the standard throttling techniques." (Office Action, Page 4).

This argument fails completely because it would be impossible to simulate processor performance states using Cooper without causing the actual ACPI state change described in Cooper. The processor in Cooper transitions between an operational ACPI state and a low power ACPI state. The claimed apparatus causes no such ACPI state change. That is the novelty of the claim. To the extent that any throttling occurred in Cooper, it would necessarily be accompanied by an ACPI state change. Therefore, Cooper, does not teach or suggest all the claim limitations as required by MPEP 2143.03 and thus the Office Action

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fails to establish a prima facie case of obviousness for claim 1. Claims 2-11 depend from claim 1 and are similarly not obvious.

Dependent Claim 10

This claim depends from claim 1 and is not obvious for at least the same reasons as its parent claim. However, claim 10 recites the additional limitation of asserting a signal on the STPCLK# line. Cooper expressly teaches away from STPCLK# throttling when it recites that "STPCLK# throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one could use Cooper to simulate processor states without causing an ACPI state change and furthermore, no-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using STPCLK# throttling. Therefore claim 10 is not obvious for this additional reason.

Independent Claim 14

Claim 14 describes a method for causing a processor to operate as though an ACPI processor performance state had been established without actually causing an ACPI processor performance state change. As described above, Cooper requires an ACPI state change. Therefore, Cooper does not render claim 14 obvious. Claims 15-21 depend from claim 14 and are similarly not obvious.

Dependent Claim 20

This claim depends from claim 14 and is not obvious for at least the same reasons as its parent claim. However, claim 20 recites the additional limitation of asserting a signal on the STPCLK# line. Cooper expressly teaches away from STPCLK# throttling when it recites that "STPCLK# throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one could use Cooper to simulate processor states

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without causing an ACPI state change and furthermore, no-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using STPCLK# throttling. Therefore claim 20 is not obvious for this additional reason.

Independent Claim 22

Claim 22 describes a computer-readable medium that stores instructions that cause a processor to perform a method. The method includes causing a processor performance state to be simulated without causing an actual ACPI state change. As described above, Cooper requires an ACPI state change. Therefore Cooper does not render claim 22 obvious.

Objection to the Specification

The Office Action objects to the disclosure because the amendment filed 3/22/07 purportedly introduced new matter. Applicant clarifies that the specification was amended on 3/22/07 solely to address the previous outstanding 35 U.S.C. §101 issues and therefore respectfully requests that this objection be removed.

Objections to the Drawings

The Office Action indicates that Figures 1-4 should be designated by a legend such as -- Prior Art -- because they purportedly illustrate only that which is old. Applicant disagrees. Figures 1 and 2, for example, include an ACPI Throttling Register 120 which, as discussed above, is not in the prior art. The ACPI specification defines a set of registers. However, none of those registers is an ACPI Throttling Register. While the ACPI standard defines registers related to system performance states, neither the ACPI standard, nor any of the references cited in the Office Action disclose an ACPI Throttling Register. Since the prior art does not disclose an ACPI throttling register, the drawings are not prior art and should not be labeled as such.

Moreover, Figures 1-8 are depictions of novel systems, methodologies, media, and other embodiments associated with simulating a processor performance state in a processor

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by manipulating an ACPI Throttling Register yet without causing an actual ACPI state change. As discussed above, the prior art does not disclose the specific throttling apparatus and methods claimed and disclosed. Therefore, Figures 1-4 are not prior art and should not be labeled as such. Applicant respectfully requests that the objections to the drawings be withdrawn.

Response to Arguments

The Office Action asserts that the language of claims 1-11 is statutory but is, nevertheless, given no patentable weight because it simply indicates an intended use. For example, the Office Action states that a "logic to select a bit pattern" is not a novel logic, but is just any logic with an intended use. This is incorrect. The recited language clearly defines how the logic is configured and how it is to function. Thus the claim recites limitations that must be given patentable weight. Also, a logic that can select a bit pattern and write the bit pattern to a specific throttling register to simulate a state change without causing a state change is a novel logic not described in any of the references. Nevertheless, Applicant has amends claims 1, 2, and 4 to make more clear that the language is not "intended use" language.

The language "configured to select a bit pattern from the set of throttling bit patterns, and to write the selected bit pattern to the ACPI throttling register to produce a simulated processor performance state without causing an actual ACPI processor performance state change" is not intended use language. Viewed correctly these words indicate structural and functional aspects of the apparatus. The language modifies "logic" to indicate the novel aspects of the logic. The limitations are not merely language to indicate what the logic will be used for but rather describe how the logic is configured to function. The Office Action asserts that the apparatus described in claims 1-11 is fully anticipated by any computer system since it is merely an apparatus with memory and logic. (Office Action, Page 9). Using this logic, no computer, no matter how unique, could ever be patentable. However, the Patent Office and the Court of Appeals for the Federal Circuit have consistently and correctly held that a general purpose computer or apparatus that is specifically configured to perform a

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specific task is patentable. Here, the general purpose elements of a memory and a logic have been given features and limitations that create a special purpose apparatus for simulating processor states without causing an ACPI state change.

The language describing how the memory is "to store an address of an ACPI (Advanced Configuration and Power Interface) throttling register in the processor and a set of throttling bit patterns to be selectively written to the ACPI throttling register" has been amended to describe a memory storing these values. This language defines limitations and is material to patentability.

Therefore, claims 1-11 do not include intended use language but rather include particular configurations and functional language that describes a novel logic and a novel memory. Therefore, claims 1-11 are not anticipated and are in condition for allowance.

Claim Interpretation

The Office Action states in a Claim Interpretation section that the claim limitation "to produce a simulated processor performance state without causing an actual ACPI processor performance state change" is being interpreted as meaning "where the actual internal frequency of the processor has not been changed (spec [0039]) by throttling a clock signal supplied to the processor (spec [0061]). While the internal state of the processor has not been changed, externally the state of the processor has changed, as the logic establishes the desired (simulated) processor performance state by causing the processor to be throttled." This interpretation does not completely make sense.

The claims specifically recite that no ACPI state change occurs. ACPI states are internal processor states that are associated with processor frequency. The interpretation provided by the Office Action makes an invalid distinction between internal ACPI states and external ACPI states. An external state simply would not be an ACPI state and therefore the interpretation lacks merit. The interpretation should be concerned with what the claims actually state (e.g., without causing an actual ACPI state change).

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Conclusion

For the reasons set forth above, **claims 1-11 and 14-22** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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